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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,783	10/06/2003	Rajneesh Jaiswal	TI-34403.1	3720

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
MCDONALD, RODNEY GLENN	

ART UNIT	PAPER NUMBER
1753	

DATE MAILED: 01/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/679,783	JAISWAL ET AL.	
	Examiner	Art Unit	
	Rodney G. McDonald	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13,14 and 16-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13,14 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Licata (U.S. Pat. 6,132,564) in view of Lane et al. (GB 2 240 875).

Licata teach that the manufacture of semiconductor devices and integrated circuits involves the blanket and selective deposition and removal of many layers of conductive, insulating, and semiconductive materials on substrates that are usually in the form of silicon wafers. The manufacturing processes typically include the formation

of a series of metal interconnect film stacks on a wafer by a plurality of sequential processes performed in a series of processing chambers of one or more multi-process vacuum processing tools. (Column 1 lines 12-19)

According to the invention cleaning is carried out by a soft sputter etch with ions of an inert gas such as argon before depositing. (Column 2 lines 59-60)

FIG. 3, for example, diagrammatically illustrates ***a semiconductor wafer processing cluster tool 100*** for carrying out certain of the embodiments of the methods described above. The tool 100 preferably includes ***a vacuum transfer module 103 (Compare to Applicant's requirement for maintaining vacuum between the reactors)*** to which are attached one or two loadlock modules 101,102 which are connected to two positions of the transfer module 103 ***having a conventional robot transfer arm 104 (Compare to Applicant's requirement for a means for advancing the wafer)*** therein. The transfer module 103 is illustrated as having three additional positions to which are attached ***processing modules 105, 106 and 107***, none of which need be a dedicated precleaning module. While only three such additional positions are illustrated, more may be provided or to one may be connected a further transfer module for transfer of substrates to other processing modules attached thereto.

In accordance with one preferred embodiment of the invention, ***the module 104 is a combined plasma pre-clean and plasma-based deposition module preferably of the type illustrated and described in connection with FIG. 2 below. The module 105 is controlled to operate, in the programmed sequence of the tool 100, as a plasma precleaning and first metal layer deposition module. (Compare to***

Applicant's first reactor for performing sputter etch) The additional modules 106 and 107 are, for example, both deposition modules. The module 106 may, for example, be a CVD module for the deposition of a second film, such as tungsten or another material that is common in semiconductor device manufacture. The Next chamber 108 may be equipped for the PVD of another material. (Compare to Applicant's requirement for providing a second reactor for depositing a layer of a metal and means for depositing a layer of metal.) This additional chamber 108 may be a chamber that could not otherwise be attached to the transfer module 103 because its position would normally be occupied by a dedicated precleaning module, which has been eliminated by the present invention.

Fig. 2 diagrammatically illustrates ***a precleaning module 10***. (See Fig. 2; Column 5 lines 62-63) ***(Compare to Applicant's first reactor for performing sputter etch)***

The module 10 includes a vacuum tight processing space 11 enclosed in a chamber 12. Mounted in the chamber 12 at one end thereof is a wafer support or susceptor 14 for supporting a semiconductor wafer 15 mounted thereon. The wafer 15, when mounted on the support 14, is parallel to and faces a target 16. The target 16 is formed of a sputter coating material, for example, titanium metal. The processing space 11 is a generally cylindrical space that it maintained at an ultra high vacuum pressure level and is filled with a processing gas, such as argon, during processing, and may include some other gas such as nitrogen. The space 11 lies in the chamber 12 between the support 14 and the target 16. (Column 6 lines 1-11)

The coil 30 inductively couples energy into process gas in the volume 26, forming an inductively coupled plasma (ICP) that generally fills the space 26. An RF generator 32, preferably operative in the range of from 0.2 to 60 MHz, for example of a frequency of 2 MHz, is connected to the coil 30 through a matching network 33 to provide the energy to the coil 30 to form the plasma in the volume 26. (Column 7 lines 26-33) ***(Compare to Applicant's requirement for providing means for producing an inductively coupled plasma adjacent to the surface of the wafer)***

Sources of processing gas 40, such as argon and nitrogen, ***are connected to the chamber 11***, through a flow control device 41. (Column 7 lines 33-35) ***(Compare to Applicant's requirement for means for passing argon to the chamber)***

In accordance with one preferred embodiment of the invention, the module 10 is operated ***to perform a plasma precleaning of the wafer 15***. In operation argon gas is maintained in the chamber 12 at approximately 10 millitorr and ICP power form the generator 32 is increased to 3.5 kWatts, while ***the substrate bias applied by the generator 27 to the substrate 15 is increased to a negative of 50 to 100 volts.*** A low power of approximately 500 to 1500 watts is applied by the power supply 20 to the target 16. (Column 9 lines 35-46) ***(Compare to Applicant's requirement for providing an RF signal to the wafer)***

The RF generator 27 operates from 0.2 to 80 MHz. (Column 9 lines 13-15) ***(Compare to Applicant's requirement for providing an RF signal to the wafer)***

As a result of such operation of the module 20, titanium is sputtered from the target 16 and is ionized in the ICP in space 26 along with atoms of the argon gas. The ions of titanium and argon are accelerated onto the substrate 15 by the bias voltage applied to the substrate. The heavier titanium ions that are included with the ions that bombard the substrate 15 ***effectively enhance the cleaning of native oxides and water vapor from the substrate surface and also react with the contaminants to reduce oxides on the surface and to dissolve oxygen into the titanium film.*** The parameters of target power, ICP power and substrate bias are maintained at a balance such that material is removed from the surface or diluted before the surface becomes covered with titanium, ***thereby performing a generally etching action***. This etching action will be carried out for a time period of approximately 20 seconds. This ionized metal etching action, while cleaning the contact 6, will result in some depositing of metal atoms 9 on the surface of the contact 6, as illustrated in FIG. 1C. (Column 9 lines 47-65)

The difference between Licata et al. and the present claims is that initially having the substrate deposited with a layer of resistor material patterned to form a plurality of nichrome resistors is not discussed.

Licata discussed above teach that semiconductor wafers can have deposited thereon layers of metal interconnect film stacks. (See Licata discussed above)

Lane et al. teach forming thin film resistors on a semi-conductor integrated circuit wafer comprising the steps of depositing a resistor layer for forming the film resistors, depositing a protective layer to define the thin film resistors, etching to remove the

protective layer in areas not protected by the photoresist, removing the photoresist, and then subjecting the wafer to radio-frequency sputter etch to remove portions of the resistor layer for defining the thin film resistors. Conductors are then formed on the wafer for connecting the thin film resistors together and to other components on the wafer. (See Abstract)

The motivation for selecting a wafer with resistors thereon is that it allows for production of a semi-conductor integrated circuit. (See Abstract)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Licata by utilizing a wafer with resistors thereon as taught by Lane because it allows for the production of a semi-conductor integrated circuit.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Licata in view of Lane et al. as applied to claims 13 and 14 above, and further in view of Bauer (U.S. Pat. 4,647,361).

The difference not yet discussed is the control of temperature during sputter etching.

Bauer teach ***sputter etching of substrates before deposition by fixing the wafer temperature in the range of approximately 350-550 degrees Centigrade***. The sputter etching can be carried out in either a double step process or single step process. The single step process utilizing the temperature of 350-550 degrees Centigrade. (Column 7 lines 29-31, lines 34-39, lines 60-68; Column 8 lines 13-18)

The motivation for sputter etching at a temperature between 350-550 degrees Centigrade is that it allows for removing oxides. (Column 7 lines 60-68; Column 8 lines 1-12)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have maintained the temperature of the wafer between 350-550 degrees Centigrade as taught by Bauer because it allows for removing oxides.

Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Licata in view of Lane et al. as applied to claims 13 and 14 above, and further in view of Lantsman (U.S. Pat. 5,589,041).

Licata discussed above teach applying a volts of 100 volts to the wafer and utilizing a RF frequency in the range of 0.2 to 80 MHz. (See Licata discussed above)

The difference not yet discussed is where the frequency applied to the inductive coil is 100 kHz is not discussed.

Lantsman teach ***sputter etching utilizing a RF power source of 0.1-27 MHz applied to the coil.*** (Column 4 lines 58-61)

The motivation for selecting a particular power to the coil is that it allows for controlling the temperature of the processing chamber. (Column 2 lines 27-31)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized an RF power to the coil of 0.1 MHz as taught by Lantsman because it allows for controlling the temperature of the processing chamber.

Response to Arguments

Applicant's arguments filed November 15, 2004 have been fully considered but they are not persuasive.

In response to the argument that Licata nor Lane does not teach means for applying an RF signal to the wafer to cause it to attract argon ions from the plasma to close to argon planes and to pinch on the service of the wafer and remove contaminated material therefrom, it is argued that Licata teach means at Column 9 lines 13-15 for providing an RF signal to the wafer in the form of a ***RF power source 27 to be applied to the wafer.*** The RF signal is provided by the RF power source 27. In operation the module 10 can be used as an ICP soft etch cleaning module by de-energizing the power supply 20 to the target 16 and, with only argon from the source 40 introduced into the chamber 12, producing an IC-plasma in the space 26 with energy from the RF generator 30 applied to the coil 60. ***The argon ions produced in the plasma in the space 26 can be accelerated toward the substrate 15 by the bias applied by the bias power supply or generator 27. These ions will strike the surface of the substrate 15 to clean the surface of the substrate.*** (See Licata Column 9 lines 23-34) The cleaning action provides the contaminant removal and the contaminant removal is discussed at Column 9 lines 47-65. (See Licata discussed above) As to the limitation of "to attract argon ions from the plasma to close argon planes to pinch on the surface of the wafer" since Licata suggest the argon ions and applicant's required power source this action is believed to take place. (See Licata discussed above)

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney G. McDonald whose telephone number is 571-272-1340. The examiner can normally be reached on M- Th with Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam X. Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Rodney G. McDonald
Primary Examiner
Art Unit 1753

RM
January 26, 2005